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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,062	06/21/2001	Marcel DeGrandpre	11585-US	4350
23553	7590	03/18/2005	EXAMINER	
MARKS & CLERK			SAM, PHIRIN	
P.O. BOX 957			ART UNIT	PAPER NUMBER
STATION B				2661
OTTAWA, ON K1P 5S7				
CANADA			DATE MAILED: 03/18/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	09/885,062	DEGRANDPRE ET AL.
	<b>Examiner</b>	<b>Art Unit</b>
	Phirin Sam	2661

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 21 June 2001.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-6 and 9-19 is/are rejected.
- 7) Claim(s) 7 and 8 is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 21 June 2001 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>06/21/2001</u> .	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
			5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
			6) <input type="checkbox"/> Other: _____ .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-6 and 9-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 6,400,718 hereinafter referred to as "Yamada" in view of US Patent 6,580,689 hereinafter referred to as "Nagai".

Yamada discloses the invention (**claim 1**) as claimed including an interface apparatus comprising:

(a) first and second devices (see Fig. 1a, elements 8 and 10), each having a series of ports for connection to a controller (see Fig. 1a, 24-34, 48-58, and 12, col. 4, lines 58-60, and col. 5, lines 4-6,12-13);

- (b) the devices operating in parallel and being configured so that when one is in an active mode the other is in a warm stand-by mode ready to become active in the event of failure of the active device (see Figs. 1a and 1b, col. 4, lines 53-58);
- (c) the ports of the device in the active mode communicating normally with the controller to initiate transfer of the packets over the packet transfer bus (see Fig. 5, col. 6, lines 53-67, col. 7, lines 1-15);
- (d) the ports of the device in the standby mode being inoperative to communicate with the controller to initiate packet transfer or to transfer packets onto the packet transfer bus, but otherwise operating normally so as to be ready for immediate activation in the event of failure of the active device (see Fig. 5, col. 7, lines 16-33).

Yamada does not disclose a common bus. However, Nagai discloses the common bus (see Fig. 2 elements 16 and 18, col. 1, lines 44-67, and col. 2, lines 1-6). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the common bus teaching by Nagai with Yamada. The motivation for doing so would have been to provide to connect to more devices and cost saving. Therefore, it would have been obvious to combine Nagai and Yamada to obtain the invention as specified in the claim 1.

**Regarding claim 2,** Yamada discloses the ports of the device in the standby mode are operative to receive from the common packet transfer bus packets whose transfer is initiated in response to a communication between the controller and the ports of the active device (see Fig. 1a, elements 2-6, 24-28, 30-34, and 12, col. 4, lines 56-67, and col. 5, lines 1-3).

**Regarding claim 3,** Yamada discloses all the limitations. On the other hand, Yamada does not disclose the common packet transfer bus is a Utopia bus. However, Nagai discloses the

Utopia bus (see Fig. 2, element 16, col. 1, lines 62-67). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the Utopia bus teaching by Nagai with Yamada. The motivation for doing so would have been to provide to bi-directional transmit and receive ATM cells simultaneously. Therefore, it would have been obvious to combine Nagai and Yamada to obtain the invention as specified in the claim 3.

**Regarding claims 4-6,** Yamada discloses all the limitations. On the other hand, Yamada does not disclose the TDM bus. However, Nagai discloses the TDM bus (see Fig. 2, element 18, col. 1, lines 44-67). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the TDM bus teaching by Nagai with Yamada. The motivation for doing so would have been to provide for static switching of synchronous traffic data between multiple devices and offers lowest complexity, a minimum and constant transmission delay, and also guarantees network bandwidth. Therefore, it would have been obvious to combine Nagai and Yamada to obtain the invention as specified in the claims 4-6.

**Regarding claim 9,** Yamada discloses an interface apparatus (see Fig. 1a) comprising:

- (a) a series of ports for connection to a controller (see Fig. 1a, elements 24-34 and 12, col. 4, lines 56-58), at least some of the ports being in an active mode (see Fig. 1a, elements 24-28) and at least some of the ports being in a standby mode (see Fig. 1a, elements 30-34);
- (b) the ports in the active and standby modes operating in parallel (see Fig. 1a, elements 24-34) and being configured so that when one is in an active mode a corresponding standby port in a warm stand-by mode ready to become active in the event of failure of the active port (see Fig. 1a, col. 4, lines 58-60);

- (c) the ports in the active mode communicating normally with the controller to initiate transfer of the packets over the packet transfer bus (see Fig. 1a, col. 4, lines 61-64);
- (d) the ports in the standby mode being inoperative to communicate with the controller to initiate packet transfer or to transfer packets onto the packet transfer bus, but otherwise operating normally so as to be ready for immediate activation in the event of failure of the corresponding active port (see Fig. 1a, col. 4, lines 65-67, col. 5, lines 1-3).

Yamada does not disclose a common packet transfer bus. However, Nagai discloses the common packet transfer bus (see Fig. 2 elements 16 and 18, col. 1, lines 44-67, and col. 2, lines 1-6). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the common bus teaching by Nagai with Yamada. The motivation for doing so would have been to provide to connect to more devices and cost saving. Therefore, it would have been obvious to combine Nagai and Yamada to obtain the invention as specified in the claim 9.

**Regarding claim 10,** Yamada discloses the ports in the standby mode are operative to receive from the common packet transfer bus packets whose transfer is initiated in response to a communication between the controller and the ports in the active mode (see Fig. 1a, elements 2-6, 24-28, 30-34, and 12, col. 4, lines 56-67, and col. 5, lines 1-3).

**Regarding claim 11,** Yamada discloses all the limitations. On the other hand, Yamada does not disclose the common packet transfer bus is a Utopia bus. However, Nagai discloses the Utopia bus (see Fig. 2, element 16, col. 1, lines 62-67). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the Utopia bus teaching by Nagai with Yamada. The motivation for doing so would have been to provide to bi-directional

transmit and receive ATM cells simultaneously. Therefore, it would have been obvious to combine Nagai and Yamada to obtain the invention as specified in the claim 11.

**Regarding claim 12,** Yamada discloses all the limitations. On the other hand, Yamada does not disclose the TDM bus. However, Nagai discloses the TDM bus (see Fig. 2, element 18, col. 1, lines 44-67). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the TDM bus teaching by Nagai with Yamada. The motivation for doing so would have been to provide for static switching of synchronous traffic data between multiple devices and offers lowest complexity, a minimum and constant transmission delay, and also guarantees network bandwidth. Therefore, it would have been obvious to combine Nagai and Yamada to obtain the invention as specified in the claim 12.

**Regarding claim 13,** Yamada discloses a method of providing redundancy in an interface apparatus for transferring data to and from a high speed packet transfer bus associated with a controller, comprising:

providing a series of ports (see Fig. 1a, elements 24-34, 48-58) configuring a redundant port operating in standby mode for each active port (see Fig. 1a, elements 30-34, col. 4, lines 65-67, and col. 5, lines 1-3), configuring the active ports to communicate normally with the controller to initiate transfer of the packets over the packet transfer bus (see Fig. , col. 4, lines 58-60, and col. 5, lines 23-26), and configuring the standby ports to be inoperative to communicate with the controller to initiate packet transfer or to transfer packets onto the bus, but otherwise to operate normally so as to be ready for immediate activation in the event of failure of a corresponding active port (see Fig. 2, col. 5, lines 57-67, col. 6, lines 1-4).

Yamada does not disclose the common packet transfer bus. However, Nagai discloses the common packet transfer bus (see Fig. 2, elements 16 or 18, col. 1, lines 44-67). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the common bus teaching by Nagai with Yamada. The motivation for doing so would have been to provide to connect to more devices and cost saving. Therefore, it would have been obvious to combine Nagai and Yamada to obtain the invention as specified in the claim 13.

**Regarding claim 14,** Yamada discloses the ports of the device in the standby mode are operative to receive from the common packet transfer bus packets whose transfer is initiated in response to a communication between the controller and the ports of the active ports (see Fig. 1a, elements 2-6, 24-28, 30-34, and 12, col. 4, lines 56-67, and col. 5, lines 1-3).

**Regarding claim 15,** Yamada discloses all the limitations. On the other hand, Yamada does not disclose the common packet transfer bus is a Utopia bus. However, Nagai discloses the Utopia bus (see Fig. 2, element 16, col. 1, lines 62-67). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the Utopia bus teaching by Nagai with Yamada. The motivation for doing so would have been to provide to bi-directional transmit and receive ATM cells simultaneously. Therefore, it would have been obvious to combine Nagai and Yamada to obtain the invention as specified in the claim 15.

**Regarding claims 16-18,** Yamada discloses all the limitations. On the other hand, Yamada does not disclose the TDM bus. However, Nagai discloses the TDM bus (see Fig. 2, element 18, col. 1, lines 44-67). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the TDM bus teaching by Nagai with Yamada. The motivation for doing so would have been to provide for static switching of synchronous traffic

data between multiple devices and offers lowest complexity, a minimum and constant transmission delay, and also guarantees network bandwidth. Therefore, it would have been obvious to combine Nagai and Yamada to obtain the invention as specified in the claims 16-18.

**Regarding claim 19,** Yamada discloses the standby ports are located on a first device in the standby mode (see Fig. 1a, elements 24-28, col. 4, lines 65-67, col. 5, lines 1-3) and the active ports are located on a second device in the active mode (see Fig. 1a, 30-34, col. 4, lines 65-67, col. 5, lines 1-3). Wherein column 4, lines 65-67 indicates when device 8 (first device) switch to standby mode which control by controller 12, then the input ports 24-28 become standby ports and device 10 (second device) become change to active mode, then the input ports 30-34 become active ports.

***Allowable Subject Matter***

4. Claims 7 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- (1) Czerwice et al (US Patent 6,687,231) discloses system and method for ensuring operations of redundant signal paths in a communication system.
- (2) Ganor et al (U.S. Patent 6,490,283) discloses communication system with communication controller and multiple physical interfaces, and method.
- (3) Tada (U.S. Patent 6,487,169) discloses cell switch module with unit cell switching function.

Art Unit: 2661

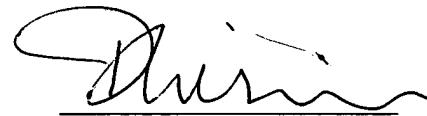
6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phirin Sam whose telephone number is (571) 272-3082. The examiner can normally be reached on Mon-Fri, 8:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau T Nguyen can be reached on (571) 272 - 3126. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Respectfully submitted,

Date: March 15, 2005



PHIRIN SAM  
PRIMARY EXAMINER